CLAIMS

What is claimed is:

1. A method for segmenting and forwarding packets, comprising:

receiving a packet, wherein the packet includes a destination that determines forwarding parameters;

as the packet is being received, creating segmentation cells from portions of the packet received, wherein each segmentation cell is provided to a switching fabric as the segmentation cell is completed;

when an end portion of the packet is received, verifying that the packet was received successfully;

when the packet has been received successfully, generating a verification data set based on segmentation cells utilized to forward the packet, wherein the verification data set is included in a final segmentation cell that is provided to the switching fabric; and

when the packet has not been received successfully, generating a purging data set that is included in the final segmentation cell that is provided to the switching fabric.

2. The method of claim 1, wherein the packet is received in a first encapsulation format, wherein at least a portion of the first encapsulation format is removed from the packet prior to creation of the segmentation cells.

3. The method of claim 2, wherein a second encapsulation format is added to the packet as the segmentation cells are created, wherein the second encapsulation format adapts the packet for transmission through the switching fabric.

4. The method of claim 1, wherein creating segmentation cells further comprises:

when a sufficient portion of the packet has been received to create a segmentation cell, creating the segmentation cell and providing the segmentation cell to the switching fabric;

storing any residual portion of the packet not included in the segmentation cell in a buffer;

combining the residual portion of the packet with subsequently received packet portions to create a subsequent segmentation cell, wherein any new residual portion of the packet resulting from creation of the subsequent segmentation cell is stored in the buffer.

5. The method of claim 4, wherein, for a first segmentation cell, determining that a sufficient portion of the packet has been received for the first segmentation cell further comprises determining that enough of the packet has been received to determine a route for segmentation cells of the packet through the switching fabric and determining that enough of the packet has been received to fill available payload space within the first segmentation cell.

6. The method of claim 4, wherein storing any residual portion of the packet further comprises:

determining a buffer location for the packet from a context table;

storing the residual portion of the packet in the buffer based on the buffer location and a current buffer count; and

updating the current buffer count to reflect storage of the residual portion in the

buffer.

7. The method of claim 6, wherein creating forwarding cells further comprises referencing the context table to determine current forwarding status of the packet.

8. The method of claim 1, wherein verifying that the packet was received successfully further comprises verifying at least one of: a received length parameter associated with the packet, and a received cyclical redundancy check parameter associated with the packet.

9. The method of claim 8, wherein generating the verification data set further comprises generating at least one of:

a verification length parameter, wherein the verification length parameter is maintained to reflect length of the packet as provided to the switching fabric as the segmentation cells are created and provided to the switching fabric such that when the final segmentation cell is created, a final value of the verification length parameter is known; and

a verification cyclical redundancy check, wherein a running cyclical redundancy check value is maintained as segmentation cells are created such that when the final segmentation cell is created a final value of the running cyclical redundancy check indicates the verification cyclical redundancy check for the packet as provided to the switching fabric.

10. The method of claim 8, wherein generating the verification data set further comprises at least one of:

modifying the received length parameter based to produce a verification length parameter that reflects length of the packet as provided to the switching fabric; and

modifying the received cyclical redundancy check parameter to produce a verification cyclical redundancy check that is valid for the packet as provided for the

switching fabric.

11. The method of claim 1, wherein receiving the packet further comprises receiving the packet as a plurality of ATM cells.

12. The method of claim 11, wherein receiving the packet as a plurality of ATM cells further comprises receiving the packet as a plurality of ATM cells over a plurality of virtual connections.

13. The method of claim 1, wherein receiving the packet further comprises receiving the packet in a packet over SONET format.

14. The method of claim 1, wherein receiving the packet further comprises receiving the packet in a Frame Relay format.

15. The method of claim 1, wherein creating segmentation cells further comprises creating fixed-length segmentation cells, wherein the switching fabric is a backplane of a fixed-transfer-length switch, wherein the backplane intercouples a plurality of fixed-transfer-length line cards, wherein the fixed-length segmentation cells facilitate forwarding packets amongst the plurality of fixed-transfer-length line cards.

16. The method of claim 1, wherein creating segmentation cells further comprises creating ATM segmentation cells, wherein the switching fabric is a backplane of an ATM switch, wherein the backplane intercouples a plurality of ATM line cards, wherein the ATM segmentation cells facilitate forwarding packets amongst the plurality of ATM line cards.

17. A segmentation and reassembly circuit, comprising:

a switching fabric;

an ingress block operably coupled to the switching fabric, wherein the ingress block receives a first packet, wherein the first packet includes a destination that determines forwarding parameters, wherein the ingress block includes:

an ingress buffer, wherein the ingress buffer stores portions of received packets, wherein each received packet has a corresponding ingress buffer index and a corresponding ingress buffer count;

an ingress context table, wherein the ingress context table stores ingress status information for at least the first packet, wherein the ingress status information includes an ingress buffer index and an ingress buffer count for the first packet;

a segmentation processor operably coupled to the ingress buffer and the ingress context table, wherein while the first packet is being received, the segmentation processor creates segmentation cells from portions of the first packet received, wherein each segmentation cell is provided to the switching fabric as it is completed, wherein when an end portion of the first packet is received, the segmentation processor verifies that the first packet was received successfully to produce a destination decision for the first packet, wherein the destination decision is included in a final segmentation cell provided to the switching fabric;

an egress block operably coupled to the switching fabric, wherein the egress block

receives the segmentation cells for the first packet from the ingress block via the switching fabric, wherein the egress block reassembles the first packet to produce a reassembled first packet from the segmentation cells, wherein the egress block forwards the reassembled first packet based on at least a portion of the forwarding parameters.

18. The circuit of claim 17, wherein the ingress status information for the first packet further includes at least one of: encapsulation configuration of the first packet, forwarding decision information for the first packet, a current ingress length for the first packet, a current ingress cyclical redundancy check value for the first packet, and a current egress cyclical redundancy check value corresponding to segmentation cells for the first packet that have been provided to the switching fabric.

19. The circuit of claim 17, wherein the egress block further comprises:

an egress buffer, wherein the egress buffer stores portions of packets being reassembled, wherein each packet being reassembled has a corresponding egress buffer index and a corresponding egress buffer count, wherein received segmentation cells for a packet being reassembled are stored in the buffer based on the corresponding egress buffer index and the corresponding egress buffer count of the packet being reassembled;

an egress context table, wherein the egress context table stores egress status information for at least the first packet, wherein the egress status information includes an egress buffer index and an egress buffer count for the first packet; and

an reassembly processor operably coupled to the egress buffer and the egress context table, wherein the reassembly processor controls storage of the segmentation cells for the first packet in the egress buffer based on the status information for the first packet in the egress context table, wherein when the first packet has been reassembled to produce a reassembled first packet and the destination decision received in the final

segmentation cell indicates that reassembled first packet is valid, the reassembly processor forwards the reassembled first packet.

20. The circuit of claim 19, wherein the reassembly processor forwards the reassembled first packet in a continuous format over an output connection.

21. The circuit of claim 19, wherein the egress status information for the first packet further includes an egress cyclical redundancy check value corresponding to the segmentation cells for the first packet that have been received from the switching fabric.

22. The circuit of claim 17, wherein the switching fabric is an ATM backplane within an ATM switch, wherein the ATM switch intercouples a plurality of line cards, wherein the ingress block is included in a first line card of the plurality of line cards, wherein the egress block is included in a second line card of the plurality of line cards.

23. The circuit of claim 16, wherein the ingress block receives packets in at least one of: an ATM cell format, a Frame Relay Format, and a packet over SONET format.

24. The circuit of claim 23, wherein ingress block removes at least a portion of framing information that is included in received packets, wherein the ingress block encapsulates segmentation cells in an internal encapsulation format that facilitates transfer of the segmentation cells across the switching fabric.

25. A segmentation circuit adapted to couple to a switching fabric, wherein the segmentation circuit receives at least a first packet, comprising:

an ingress buffer, wherein the ingress buffer stores portions of received packets, wherein each received packet has a corresponding ingress buffer index and a corresponding ingress buffer count;

an ingress context table, wherein the ingress context table stores ingress status information for at least the first packet, wherein the ingress status information includes an ingress buffer index and an ingress buffer count for the first packet; and

a segmentation processor operably coupled to the ingress buffer and the ingress context table, wherein while the first packet is being received, the segmentation processor creates segmentation cells from portions of the first packet received, wherein each segmentation cell is provided to the switching fabric as it is completed, wherein when an end portion of the first packet is received, the segmentation processor verifies that the first packet was received successfully to produce a destination decision for the first packet, wherein the destination decision is included in a final segmentation cell provided to the switching fabric.

26. The circuit of claim 25, wherein the segmentation processor determines when a sufficient portion of the first packet has been received to create a first segmentation cell, wherein the first segmentation cell includes internal framing information and a first payload, wherein the first payload includes a first portion of the first packet, wherein size of the first portion is based on size of the internal framing information such that the first segmentation cell is filled.

27. The circuit of claim 26, wherein the segmentation processor creates segmentation cells as sufficient portions of the first packet are received, wherein any residual received

portion remaining after creation of a segmentation cell is stored in the ingress buffer such that it is available for combination with subsequent received portions to create subsequent segmentation cells.

28. The circuit of claim 27, wherein the ingress status information for the first packet further includes at least one of: encapsulation configuration of the first packet, forwarding decision information for the first packet, a current ingress length for the first packet, a current ingress cyclical redundancy check value for the first packet, and a current egress cyclical redundancy check value corresponding to segmentation cells for the first packet that have been provided to the switching fabric.

29. A segmentation processor for forwarding a packet that is received, wherein the packet includes a destination that determines forwarding parameters, comprising:

a processing module; and

memory operably coupled to the processing module, wherein the memory stores operating instructions that, when executed by the processing module, cause the processing module to perform the functions of:

as the packet is being received, creating segmentation cells from portions of the packet received, wherein each segmentation cell is provided to a switching fabric as the segmentation cell is completed;

when an end portion of the packet is received, verifying that the packet was received successfully;

when the packet has been received successfully, generating a verification data set based on segmentation cells utilized to forward the packet, wherein the verification data set is included in a final segmentation cell that is provided to the switching fabric; and

when the packet has not been received successfully, generating a purging data set that is included in the final segmentation cell that is provided to the switching fabric.

30. The segmentation processor of claim 29, wherein the packet is received in a first encapsulation format, wherein the memory includes operating instructions that, when executed by the processing module, cause the processing module to remove at least a portion of the first encapsulation format from the packet prior to creation of the segmentation cells.

31. The segmentation processor of claim 30, wherein the memory includes operating instructions that, when executed by the processing module, cause the processing module to add a second encapsulation format to the packet as the segmentation cells are created, wherein the second encapsulation format adapts the packet for transmission through the switching fabric.

32. The segmentation processor of claim 29, wherein the memory includes operating instructions that, when executed by the processing module, cause the processing module to perform the function of creating segmentation cells such that creating segmentation cells further comprises:

when a sufficient portion of the packet has been received to create a segmentation cell, creating the segmentation cell and providing the segmentation cell to the switching fabric;

storing any residual portion of the packet not included in the segmentation cell in a buffer;

combining the residual portion of the packet with subsequently received packet portions to create a subsequent segmentation cell, wherein any new residual portion of the packet resulting from creation of the subsequent segmentation cell is stored in the buffer.

33. The segmentation processor of claim 32, wherein the memory includes operating instructions that, when executed by the processing module, cause the processing module to perform the function of creating segmentation cells such that, for a first segmentation cell, determining that a sufficient portion of the packet has been received for the first segmentation cell further comprises determining that enough of the packet has been

received to determine a route for segmentation cells of the packet through the switching fabric and determining that enough of the packet has been received to fill available payload space within the first segmentation cell.

34. The segmentation processor of claim 29, wherein the memory includes operating instructions that, when executed by the processing module, cause the processing module to perform the function of storing any residual portion of the packet such that storing any residual portion of the packet further comprises:

determining a buffer location for the packet from a context table;

storing the residual portion of the packet in the buffer based on the buffer location and a current buffer count; and

updating the current buffer count to reflect storage of the residual portion in the buffer.

35. The segmentation processor of claim 34, wherein the memory includes operating instructions that, when executed by the processing module, cause the processing module to perform the function of creating forwarding cells such that creating forwarding cells further comprises referencing the context table to determine current forwarding status of the packet.

36. The segmentation processor of claim 29, wherein the memory includes operating instructions that, when executed by the processing module, cause the processing module to perform the function of verifying that the packet was received successfully such that verifying further comprises verifying at least one of: a received length parameter associated with the packet, and a received cyclical redundancy check parameter associated with the packet.

37. The segmentation processor of claim 36, wherein the memory includes operating instructions that, when executed by the processing module, cause the processing module to perform the function of generating the verification data set such that generating the verification data set further comprises generating at least one of:

a verification length parameter, wherein the verification length parameter is maintained to reflect length of the packet as provided to the switching fabric as the segmentation cells are created and provided to the switching fabric such that when the final segmentation cell is created, a final value of the verification length parameter is known; and

a verification cyclical redundancy check, wherein a running cyclical redundancy check value is maintained as segmentation cells are created such that when the final segmentation cell is created a final value of the running cyclical redundancy check indicates the verification cyclical redundancy check for the packet as provided to the switching fabric.

38. The segmentation processor of claim 36, wherein the memory includes operating instructions that, when executed by the processing module, cause the processing module to perform the function of generating the verification data set such that generating the verification data set further comprises at least one of:

modifying the received length parameter based to produce a verification length parameter that reflects length of the packet as provided to the switching fabric; and

modifying the received cyclical redundancy check parameter to produce a verification cyclical redundancy check that is valid for the packet as provided for the switching fabric.

39. The segmentation processor of claim 29, wherein the packet is received as a plurality of ATM cells.

40. The segmentation processor of claim 39, wherein the packet is received as a plurality of ATM cells over a plurality of virtual connections.

41. The segmentation processor of claim 29, wherein the packet is received in a packet over SONET format.

42. The segmentation processor of claim 29, wherein the packet is received in a Frame Relay format.

43. The segmentation processor of claim 29, wherein the memory includes operating instructions that, when executed by the processing module, cause the processing module to perform the function of creating segmentation cells such that creating segmentation cells further comprises creating fixed-length segmentation cells, wherein the switching fabric is a backplane of a fixed-transfer-length switch, wherein the backplane intercouples a plurality of fixed-transfer-length line cards, wherein the fixed-length segmentation cells facilitate forwarding packets amongst the plurality of fixed-transfer-length line cards.

44. The segmentation processor of claim 29, wherein the memory includes operating instructions that, when executed by the processing module, cause the processing module to perform the function of creating segmentation cells such that creating segmentation cells further comprises creating ATM segmentation cells, wherein the switching fabric is a backplane of an ATM switch, wherein the backplane intercouples a plurality of ATM line cards, wherein the ATM segmentation cells facilitate forwarding packets amongst the plurality of ATM line cards.